Introduction:

In the rapidly evolving landscape of radio communications, high-performance receivers are essential for ensuring reliable and accurate signal processing across a wide range of frequencies. The AR5700D digital communications receiver represents a significant advancement in this domain, offering a sophisticated architecture designed to meet the demanding requirements of modern signal detection and processing. This document delves into the intricate design and operational features of the AR5700D, exploring its innovative signal flow mechanisms, image reception suppression techniques, and advanced digital signal processing capabilities. By examining the key components and their roles within the receiver's architecture, we aim to provide a comprehensive understanding of how the AR5700D achieves exceptional performance, particularly in challenging environments where precision and consistency are paramount.

1. Signal Flow and Processing Stages in the AR5700D Receiver

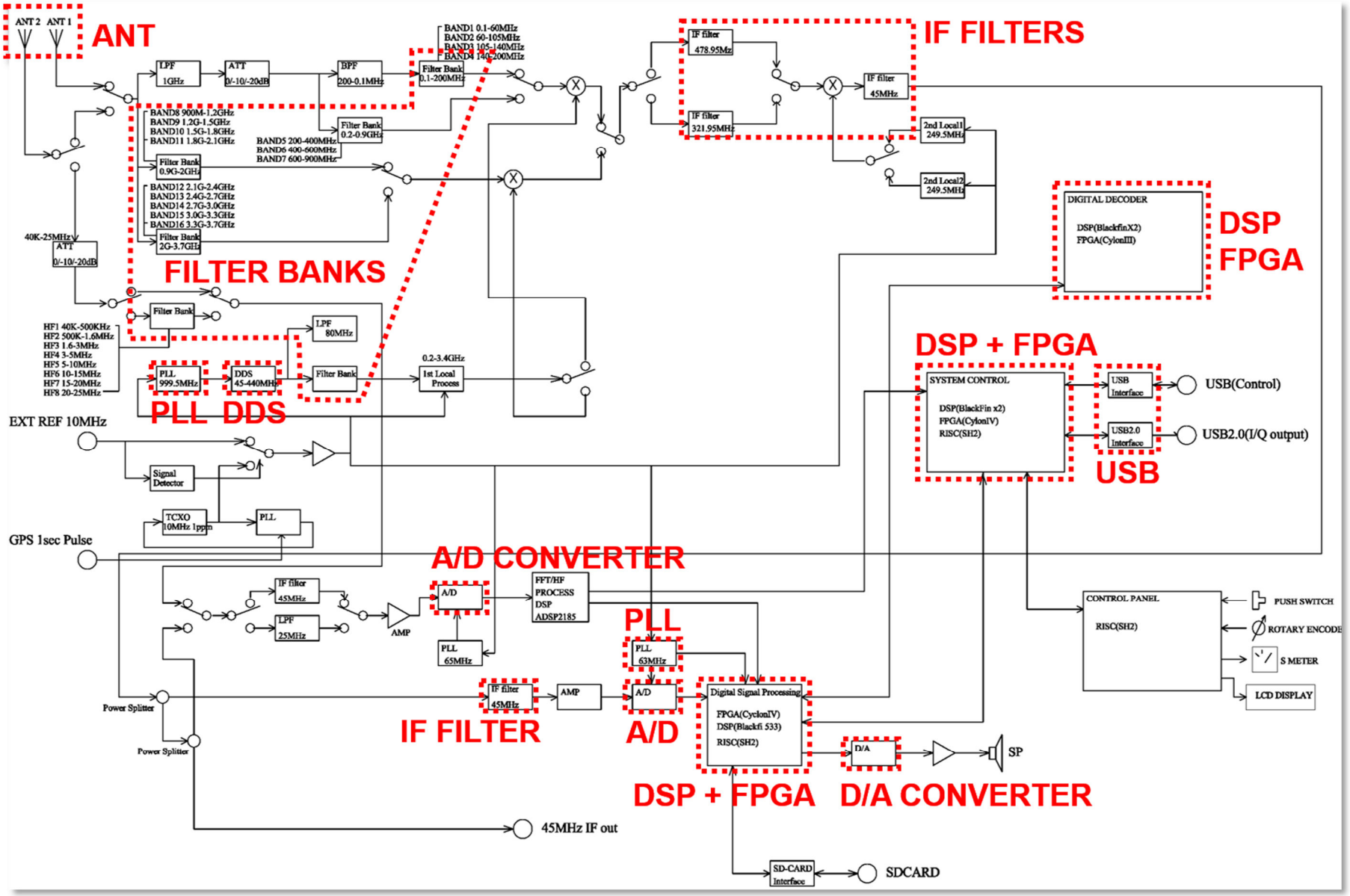
The following signal flow chart of the AR5700D receiver illustrates the signal processing stages from the antenna input to the final output. Key stages include various filter banks, local oscillators, signal detection, and digital signal processing.

Key Components and Signal Paths:

- **ANT 1 and ANT 2:** Antenna inputs connected to filter banks.
- **Filter Banks:** Multiple filter banks process different frequency bands, from 0.1 MHz to 3.7 GHz.
- **PLL and DDS:** Phase-Locked Loops (PLLs) and Direct Digital Synthesizers (DDS) generate stable local oscillator signals for mixing stages.
- **IF Filters:** Intermediate Frequency (IF) filters at various stages (45 MHz, 321.95 MHz, and 478.95 MHz) for image suppression.
- **A/D and D/A Converters:** Analog-to-Digital and Digital-to-Analog converters for signal digitization and processing.
- **DSP and FPGA:** Digital Signal Processing (DSP) and Field-Programmable Gate Arrays (FPGA) for advanced signal processing and system control.
- **USB Interface:** For data transfer and control signal interfacing.

This flow chart serves as a visual guide to the signal processing stages and the integration of various components, which are elaborated upon in the subsequent sections of this article.

Figure 1: Signal flown diagram

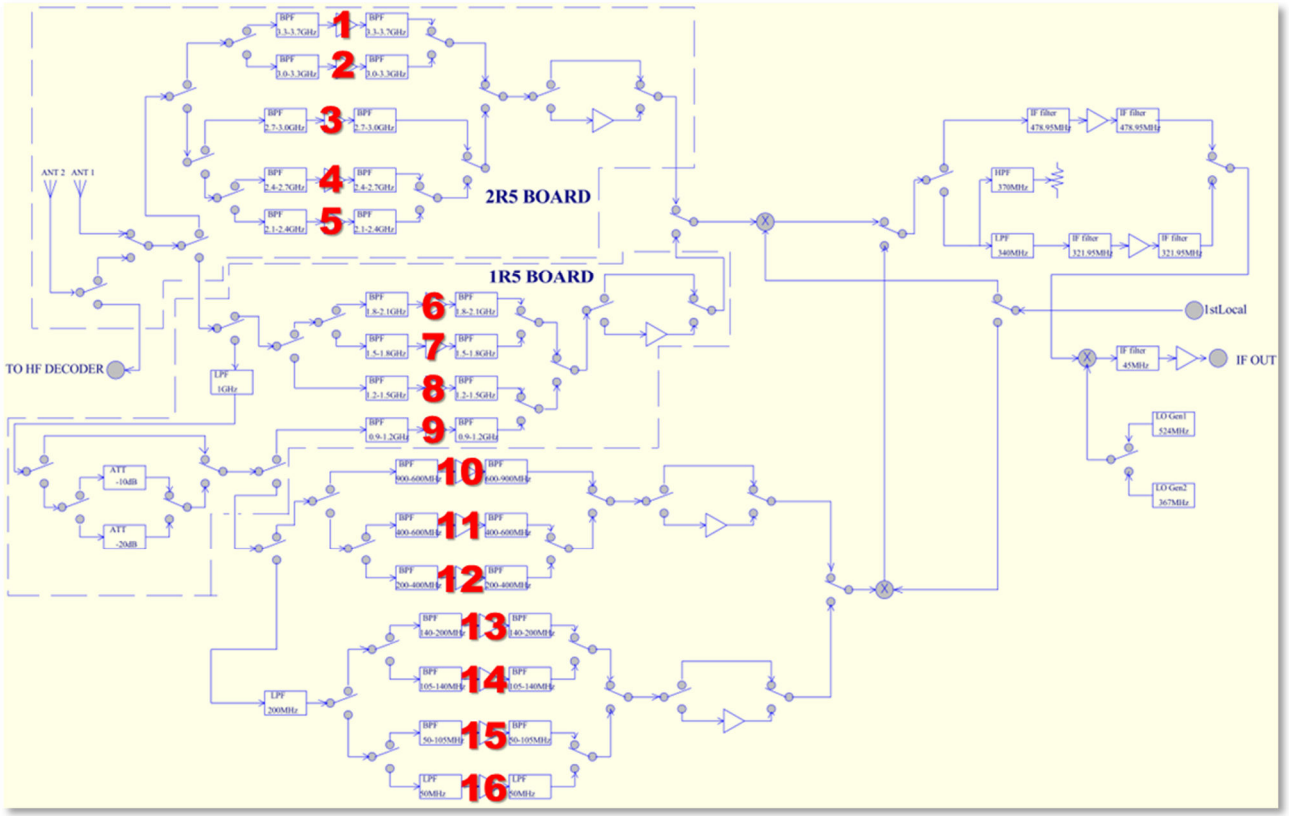


2. Eliminating Image Reception Effectively

A significant challenge in superheterodyne receivers is the interference caused by image reception from spurious signals. Image reception occurs when the received signal frequency (Fs), the first Intermediate Frequency (Fif), and the local oscillator frequency (Fl) interact such that Fif(l) = Fl - Fs or Fif(u) = Fs + Fl. To counteract this, if Fif is selected as Fif(l), Fif(u) represents the unwanted image frequency, and vice versa. To mitigate this issue, a robust front-end filter bank is implemented immediately after the antenna input to exclude these unwanted signals.

In the double superheterodyne configuration, the first IF frequencies are set at 321.95 MHz and 478.95 MHz, with a second IF at 45.05 MHz. To ensure comprehensive suppression of image reception, the incoming signal undergoes filtration through a 16-band filter bank, configured as follows:

Figure 2: RF Front-End diagram



1	3,300 MHz to 3,700 MHz
2	3,000 MHz to 3,300 MHz
3	2,700 MHz to 3,000 MHz
4	2,400 MHz to 2,700 MHz
5	2,100 MHz to 2,400 MHz
6	1,800 MHz to 2,100 MHz
7	1,500 MHz to 1,800 MHz
8	1,200 MHz to 1,500 MHz
9	900 MHz to 1,200 MHz
10	600 MHz to 900 MHz
11	400 MHz to 600 MHz
12	200 MHz to 400 MHz
13	140 MHz to 200 MHz
14	105 MHz to 140 MHz
15	50 MHz to 105 MHz
16	50 MHz (LPF)

The use of lower IF frequencies requires precise division into specific frequency bands, particularly above 2.1 GHz, where the complexity of microwave filter design increases. Frequencies below 25 MHz utilize direct sampling with A/D conversion, followed by digital demodulation.

The filter bank circuits are encased within a die-cast shield.

Figure 3: Die-cast shield

Opening this shield reveals five filter banks for the 2.1 GHz to 3.7 GHz range, each with a 300 MHz bandwidth, designed using a two-stage interdigital filter with a Low Noise Amplifier (LNA) constructed from microstrip lines.

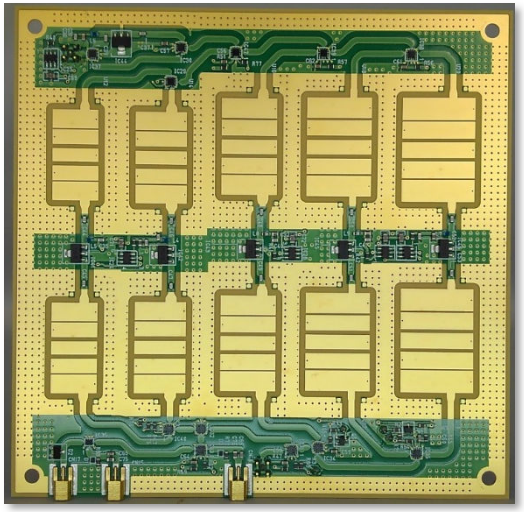


Figure 4: 2.1~3.7GHz filter banks

Upon further disassembly, another layer under the top filter board contains four filter banks for the 900 MHz to 2.1 GHz range, also featuring a 300 MHz bandwidth. This layer primarily employs LC filters with inductors and capacitors constructed using microstrip technology in a two-stage configuration.

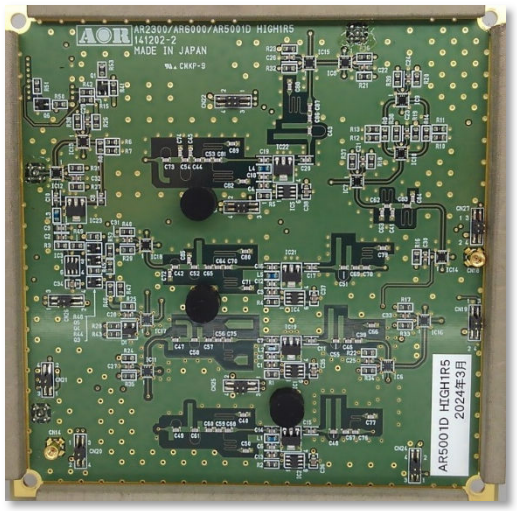


Figure 5: 0.9~2.1GHz filter banks

Removing this layer exposes the final seven bands of the front-end, spanning from 25 MHz to 900 MHz.

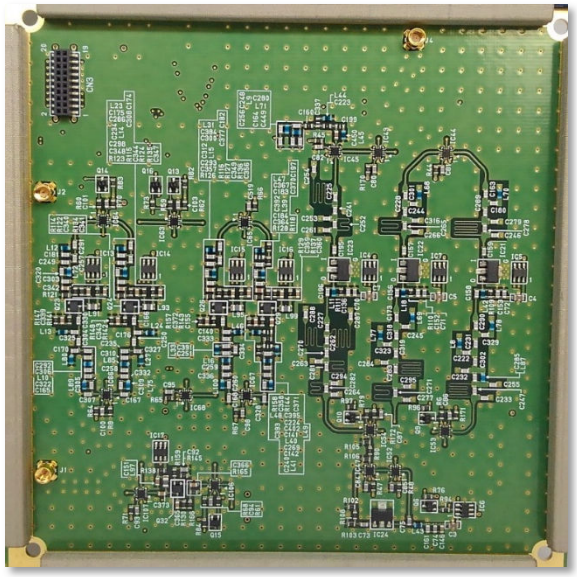


Figure 6: 25~900MHz filter banks

The three highest bands cover 600 MHz to 900 MHz, 400 MHz to 600 MHz, and 200 MHz to 400 MHz, with inductors again realized using microstrip lines.

Each filter in the front-end is meticulously designed to provide optimal passband characteristics and cutoff properties for effective image suppression, aiming for an image suppression ratio of at least 60 dB across all bands.

Confirmatory tests have shown that the image suppression characteristics for each band consistently achieve or exceed this 60 dB threshold.

Receiving frequency	IF level	Image level	Suppression ratio	1st IF frequency
25MHz	-33.2dBm	- 124.3dBm	91.1dB	321.95MHz
320MHz	-32.5dBm	- 107.0dBm	74.5dB	478.95MHz
2GHz	-32.8dBm	- 109.5dBm	76.7dB	478.95MHz
3GHz	-33.5dBm	-115.9dBm	82.4dB	478.95MHz
3.6GHz	-32.7dBm	-116.4dBm	83.7dB	478.95MHz

3. High C/N First Local Signal via DDS, Rapid Switching, and Low Noise Floor

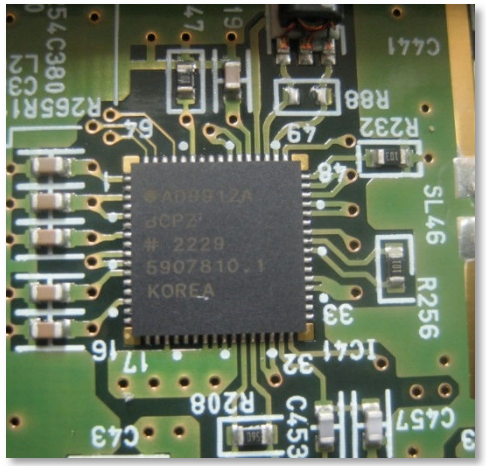


Figure 7: The DDS clock synthesizer AD9912

In high-performance receivers like the AR5700D, the C/N (Carrier to Noise) ratio and the phase noise of the IF signal are crucial. These factors significantly affect the receiver's sensitivity and its ability to suppress adjacent interference. A high noise floor in the local signal hampers achieving optimal sensitivity suppression. Furthermore, the ability to quickly search and stabilize upon frequency changes is essential for identifying unknown signals efficiently.

Traditional frequency synthesizers combine a VCO (Voltage Controlled Oscillator) and a PLL (Phase Locked Loop) to generate local signals. However, achieving low phase noise and rapid frequency switching simultaneously is challenging due to the inherent limitations of VCOs and the discrete nature of PLL frequency steps. To overcome these issues, the AR5700D employs a 1 GHz DDS (Direct Digital Synthesizer), the AD9912, as part of the PLL's reference signal to enable smoother frequency transitions.

A critical challenge with using DDS technology is the occurrence of spurious signals, which are difficult to mitigate due to the fundamental operation principles of DDS. The AD9912, however, includes an advanced spurious signal cancellation circuit that effectively reduces these unwanted signals, which are otherwise tough to filter out.

The phase noise of the DDS's clock source directly impacts the output's phase noise. To address this, the AR5700D uses a PLL with a coaxial-type ceramic resonator VCO to generate a high C/N, high-purity clock signal.

Despite its capabilities, a 1 GHz DDS alone cannot cover all the local signal frequencies required by the AR5700D, which range from 200 MHz to 3.4 GHz. While the spurious canceller addresses some issues, additional spurious signals at higher frequencies are managed using frequency multipliers and extensive filtering. A Variable Gain Amplifier (VGA) is also implemented to adjust signal levels consistently across different frequencies. These components are integrated into the FILTER board's processing circuitry, where numerous microstrip filters were utilized.

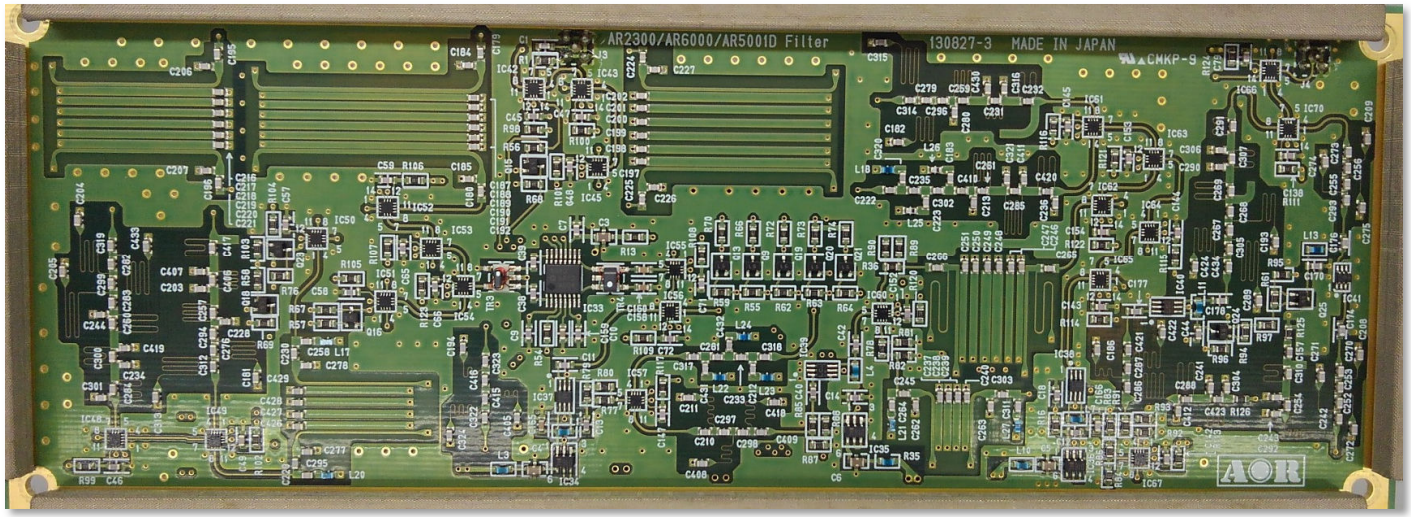
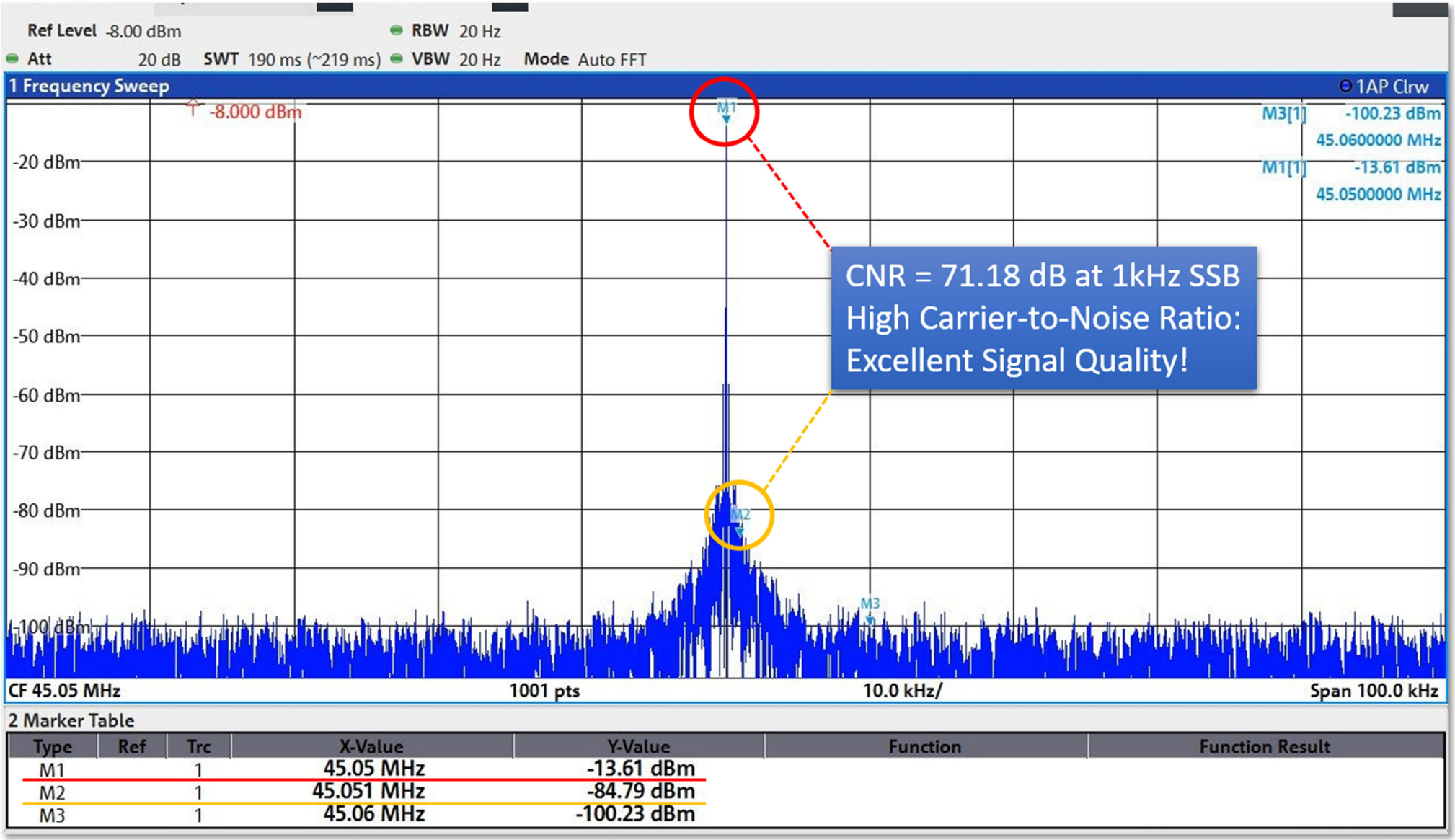


Figure 8: Filter board

The AR5700D features a double superheterodyne architecture. The quality of the local oscillator that converts the first IF to the second IF at 45.05 MHz critically influences the IF output. For stability and high C/N ratio, the second local oscillator uses a crystal oscillator fixed at 367 MHz and 524 MHz.

To illustrate the robust performance characteristics, a spectrum analysis of the 45.05 MHz IF output when receiving a 25 MHz/-30 dBm signal is displayed here, demonstrating the effectiveness of these design choices.

Figure 9: IF-OUT spectrum



4. Wide IF Output with Low Distortion and Minimal Harmonic Spur

A defining characteristic of the AR5700D receiver is its ability to deliver a 45.05 MHz IF output directly from the antenna with minimal spurious emissions and low distortion. The IF bandwidth is maintained at 15 MHz. Unlike other receivers that utilize traditional AGC (Automatic Gain Control) circuits, which can be detrimental to performance, the AR5700D avoids these. The IIP3 (Input Third-Order Intercept Point) at the IF output remains exceptionally high, exceeding 6 dB, while preserving the sensitivity that is characteristic of conventional receivers. Utilizing AGC to manage weak signals would risk distorting stronger, unwanted signals within the same 15 MHz bandwidth. Therefore, AGC is not a viable solution for signal processing in this context.

So, how does the AR5700D manage signal integrity? The key lies in bypassing AGC altogether. The IF signal output is directly digitized using an A/D converter, eliminating the distortions typically associated with analog gain control. Subsequent signal processing tasks, such as filtering and dynamic range management, are handled by sophisticated, proprietary digital signal processing techniques. This approach essentially transforms the receiver into an SDR (Software Defined Radio), ensuring high-performance reception and processing.

The AR5700D receiver's design also places a strong emphasis on minimizing unwanted spurious signals to enhance signal integrity and overall performance. Harmonic spurs, which are unwanted frequencies generated as a byproduct of signal processing, pose a significant challenge in maintaining signal fidelity, especially in high-performance receivers like the AR5700D.

Harmonic Spur Reduction Techniques

The AR5700D leverages the capabilities of the AD9912 DDS (1 GSPS Direct Digital Synthesizer with 14-Bit DAC) to address the issue of harmonic spurs effectively. The AD9912 is equipped with advanced features designed specifically for spur reduction, which are critical in achieving the high signal purity required in demanding communication environments.

SpurKiller Technology

One of the key features of the AD9912 utilized in the AR5700D is its dual-channel SpurKiller technology. This technology is specifically designed to reduce harmonic spurs generated during the digital synthesis process. The SpurKiller operates by applying an optimized correction to the output signal, effectively reducing the amplitude of specific spurious signals. This correction is achieved through careful adjustment of internal parameters, which are dynamically configured based on the desired output frequency.

Harmonic Spur Correction Process

The harmonic spur correction process within the AD9912 involves a series of steps aimed at minimizing the impact of unwanted harmonics.

Identification of Harmonic Spurs: The AD9912 identifies potential harmonic spurs based on the selected output frequency and system clock characteristics. The SpurKiller channels are then configured to target these specific spurs.

Dynamic Correction: Once identified, the SpurKiller applies a dynamic correction to the DDS output. This correction is fine-tuned to minimize the spur amplitude, often achieving suppression levels that are sufficient to render the spurs negligible in the receiver's final output.

Calibration and Optimization: The AR5700D receiver undergoes a calibration process during manufacturing, where the DDS settings, including those related to spur reduction, are optimized for each unit. This ensures that the harmonic spur reduction is tailored to the specific characteristics of the receiver, further enhancing performance.

Impact on Receiver Performance

The effective reduction of harmonic spurs directly contributes to the AR5700D's ability to maintain a high Carrier-to-Noise (C/N) ratio and low phase noise, which are critical parameters for signal clarity and receiver sensitivity. By integrating the AD9912's SpurKiller technology, the AR5700D achieves a significant reduction in spurious emissions, leading to cleaner signals and improved performance across its wide operational frequency range.

5. Consistent Gain from Antenna to IF Output

In most receivers, the gain from the antenna signal to the IF output tends to fluctuate across different frequencies due to the various circuits it passes through. However, the AR5700D takes advantage of not using AGC (Automatic Gain Control) to enhance consistency. Before they leave the factory, each AR5700D receiver undergoes individual calibration. This meticulous process ensures that the gain from the antenna to the A/D (Analog-to-Digital Converter) input is maintained within a tight range of 30 dB ± 3 dB, thereby achieving uniform performance across all units.

The calibration process utilizes a signal generator, a PC with dedicated software, and programming of the digital gain control calibration flash memory.

1. Signal Generator (SG): The signal generator (N5171B) is used to provide a highly accurate and stable signal across a wide frequency range (25 MHz to 3.7 GHz) at a defined level. This input signal is essential for testing and calibrating the receiver’s response.
2. Receiver Configuration: The AR5700D receiver is configured with various filter banks that cover different frequency bands. The calibration process requires measuring each of these bands individually in chunks of 10MHz. The frequency bands range from 0.1 MHz to 3.7 GHz, divided into smaller sub-bands, each filtered and processed through the receiver's signal chain.
3. PC with Dedicated Software: A PC running specialized software interfaces with the receiver via USB. This software controls the signal generator and the receiver, automating the calibration process. It is responsible for programming the digital gain control settings into the receiver's flash memory.

4. Calibration Flash Memory (CAL): The calibration data, which includes digital gain control settings, is stored in a dedicated flash memory module within the receiver. This memory is programmed during the calibration process and precisely programs the variable gain amplifier (VGA) for precision gain control, high IP3 and very low noise.

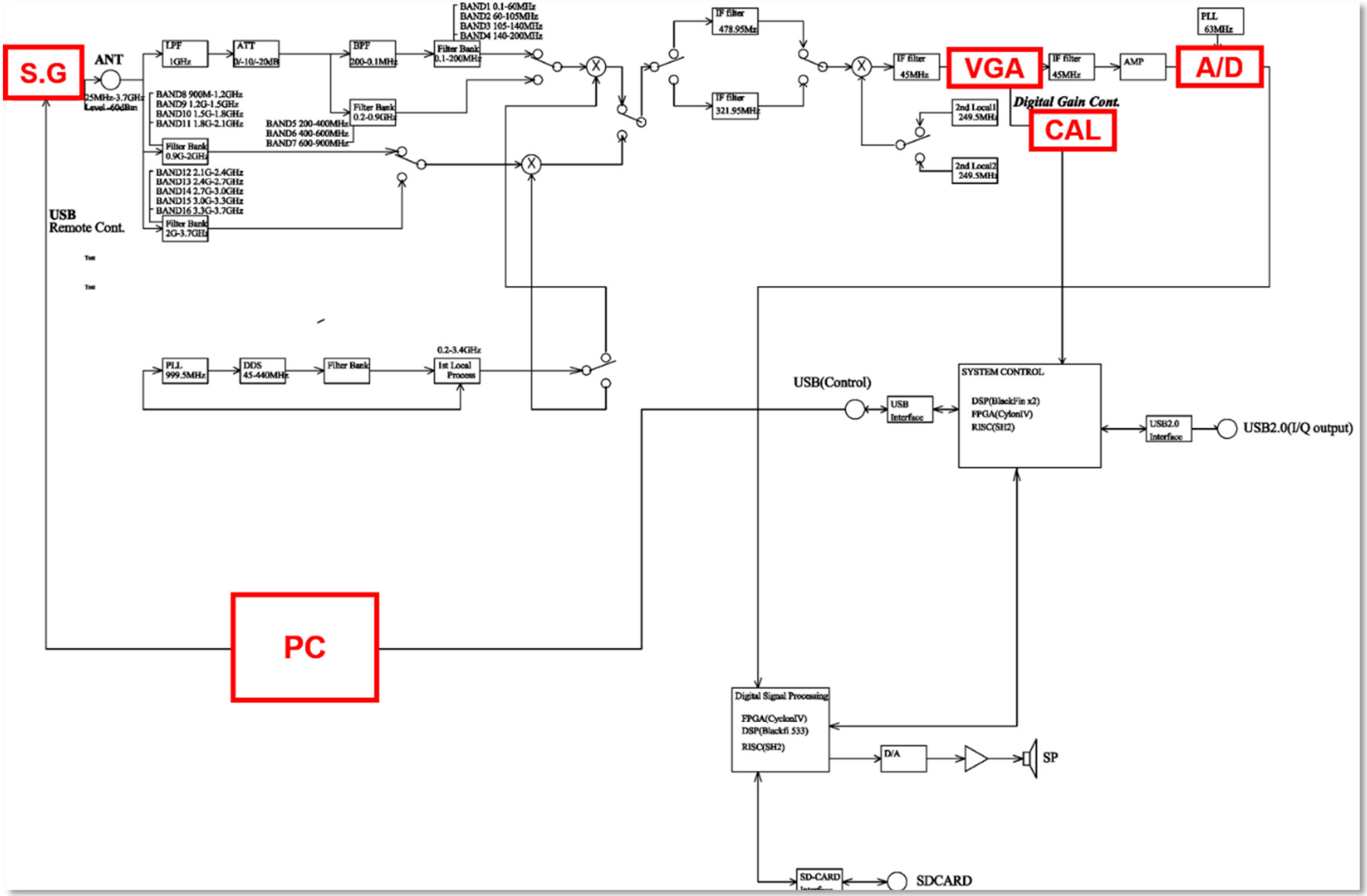


Figure 10: Frequency response calibration method

Applicability:

The technology described in this document for the AR5700D also apply to our AR2300, AR5001D, and AR6000 receivers. These products share similar advanced features and design philosophies, ensuring consistent performance across our range of high-performance receivers.

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